STACKED SEMICONDUCTOR CHIP PACKAGE

BACKGROUND OF THE INVENTION

1. Field of the invention

The present invention relates to a semiconductor chip package, more particularly, to a stacked semiconductor chip package.

2. Description of the Related Art

Referring to Figs. 1a and 1b, the conventional stacked semiconductor chip package 1 comprises a substrate 11, a first chip 12, a plate 13, and a second chip 14. The first chip 12 adheres to the substrate 11 and electrically connects to the substrate 11 by a plurality of leads. The plate 13 is mounted between the first chip 12 and the second chip 14. The size of the plate 13 is usually smaller than that of the first chip 12 so as to avoid interfering the connection of the first chip 12 and the substrate 11.

The plate 13 adheres to the first chip 12 by using an adhesive. The second chip 14 is mounted on the plate 13, and adheres to the plate 13 by using an adhesive. Referring to Fig. 1b, because the size of the second chip 14 is larger than that of the plate 13, the testing instrument cannot detect the thickness of the adhesive layer 15 and the size of the overflow adhesive portion 16. If the adhesive layer 15 is too thin or the overflow adhesive portion 16 is too large, the adhesive on the overflow adhesive portion 16 will be broken so that the second chip 14 cannot exactly adhere to the plate 13, which will cause the semiconductor chip package product failure.

Therefore, it is necessary to provide an innovative and progressive semiconductor chip package so as to solve the above problem.

SUMMARY OF THE INVENTION

One objective of the present invention is to provide a stacked semiconductor chip package comprising a substrate, a first chip, a plate, and a second chip. The first chip is mounted on the substrate and electrically connects to the substrate by a plurality of electrical leads. The second chip electrically connects to the substrate by a plurality of electrical leads and has two opposed longitudinal sides defining a first length. The plate is mounted between the first chip and the second chip and connects the first chip and the second chip. Corresponding to the two longitudinal sides of the second chip, the plate has two opposed longitudinal sides defining a second length. The second length is larger than the first length to expose the opposed longitudinal sides of the plate. An overflow adhesive portion is formed between the plate and the second chip, and the overflow adhesive portion exposes on the plate. Therefore, the testing instrument can detect the size of the overflow adhesive portion and the thickness of the adhesive layer so as to control the quality of the stacked semiconductor chip package. The adhesion strength between the second chip and the plate can be augmented to raise the reliability of the stacked semiconductor chip package product.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1a shows a front and cross-sectional view, according to the conventional stacked semiconductor chip package;

Fig. 1b shows a top plan view, according to the conventional stacked semiconductor chip package;

Fig. 2a shows a front and cross-sectional view, according to the first embodiment of the invention;

Fig. 2b shows a top plan view, according to the first embodiment of the invention;

Fig. 2c shows a side and cross-sectional view, according to the first embodiment of the invention;

Fig. 3a shows a front and cross-sectional view, according to the second embodiment of the invention;

Fig. 3b shows a top plan view, according to the second embodiment of the invention; and

Fig. 3c shows a side and cross-sectional view, according to the second embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

Referring to Figs. 2a, 2b, and 2c, according to the first embodiment of the invention, the stacked semiconductor chip package 2 comprises a substrate 21, a first chip 22, a plate 23, and a second chip 24. The first chip 22 is mounted on the substrate 21 and electrically connects to the substrate 21 by a plurality of electrical leads. The plate 23 is mounted between the first chip 22 and the second chip 24, and is stacked on the first chip 22. The plate 23 adheres to the first chip 22 by using an adhesive.

The second chip 24 is mounted on the plate 23, and adheres to the plate 23 by using an adhesive. Referring to Fig. 2b, the second chip 24 has two opposed longitudinal sides defining a first length L1. Corresponding to the two longitudinal sides of the second chip 24, the plate 23 has two opposed longitudinal sides defining a second length L2. The second length L2 is larger than the first length L1 to expose the opposed longitudinal sides of the plate 23. An overflow adhesive portion 26 is formed between the plate 23 and the second chip 24, and the overflow adhesive portion 26 exposes on the plate 23. Therefore, the testing instrument can detect the size of the overflow adhesive portion 26 and the thickness of the adhesive layer 25 so as to control the quality of the stacked semiconductor chip package. The adhesion strength between the second chip 24 and the plate 23 can be augmented to raise the reliability of the stacked semiconductor chip package product.

According to the first embodiment of the invention, the size of the first

chip 22 is substantially identical with that of the second chip 24. The plate 23 should not entirely cover the first chip 22 so as to have enough space for connecting the first chip 22 and the substrate 21. Corresponding to the two longitudinal sides of the second chip 24, the first chip 22 and the second chip 24 respectively further have two opposed transverse sides defining a first width W1. The plate 23 further has two opposed transverse sides defining a second width W2. The second width W2 is smaller than the first width W1 so as to have enough space for connecting the first chip 22 and the substrate 21.

As shown in Figs. 3a, 3b, and 3c, according to the second embodiment of the invention, the stacked semiconductor chip package 3 comprises a substrate 31, a first chip 32, a plate 33, and a second chip 34. The structure of the stacked semiconductor chip package 3 of the second embodiment is similar to that of the stacked semiconductor chip package 2 of the first embodiment. The difference between the package 3 and the package 2 is the size of the first chip 32, the plate 33, and the second chip 34.

Referring to Fig. 3b, the second chip 34 has two opposed longitudinal sides defining a first length L4. Corresponding to the two longitudinal sides of the second chip 34, the plate 33 has two opposed longitudinal sides defining a second length L5. The second length L5 is larger than the first length L4 to expose the opposed longitudinal sides of the plate 33. An overflow adhesive portion 36 is formed between the plate 33 and the second chip 34, and the overflow adhesive portion 36 exposes on the plate 33. Therefore, the testing instrument can detect the size of the overflow adhesive portion 36 and the thickness of the adhesive layer 35 so as to control the quality of the stacked semiconductor chip package 3.

Corresponding to the two longitudinal sides of the second chip 34, the first chip 32 has two opposed longitudinal sides defining a third length L6. The third length L6 is larger than the second length L5 so as to have enough space for connecting the first chip 32 and the substrate 31 by using

the leads on the opposed longitudinal sides of the first chip 32.

Furthermore, corresponding to the two longitudinal sides of the second chip 34, the second chip 34 further has two opposed transverse sides defining a first width W4. The plate 33 further has two opposed transverse sides defining a second width W5. The first chip 32 further has two opposed transverse sides defining a third width W6. The second width W5 is smaller than the first width W4 and the third width W6 so as to have enough space for connecting the first chip 32 and the substrate 31 by using the leads on the opposed transverse sides of the first chip 32.

As the embodiments of the present invention have been illustrated and described, various modifications and improvements can be made by those skilled in the art. The embodiments of the present invention are therefore described in an illustrative but not restrictive sense. It is intended that the present invention may not be limited to the particular forms as illustrated, and that all modifications which maintain the spirit and scope of the present invention are within the scope as defined in the appended claims.